IN THE SPECIFICATION:

Please insert before the first paragraph under BACKGROUND OF THE INVENTION of page 1 of the disclosure currently on file with the following paragraph:

This application is a Continuation application of U.S. Application No. 10/051,188 filed on January 22, 2002. Priority is claimed based on U.S. Application No. 10/051,188 filed on January 22, 2002.

Please replace the last paragraph of page 14 (continuing to page 15) of the Disclosure currently on file with the following paragraph:

Referring next to Figure 7B, the vertical Source-Channel-Drain columns (S-C-D) of the [[P]]NMOS transistors Q3, Q4 are formed as follows. A first poly-silicon source layer 38-1 (doped with an n-type impurity, ex. P, As), a first poly-silicon channel layer 40-1 (doped with an p-type impurity, ex. B, BF_2), and a first poly-silicon drain layer 39-1 (doped with an n-type impurity, ex. P, As) are deposited in sequence by a CVD method. It is also possible to form the first poly-silicon source layer 38-1, the first poly-silicon channel layer 40-1, and the first poly-silicon drain layer 39-1 by ion-implanting. A first mask layer (completely removed later so it is not shown in the final structure of Figure 7B) is deposited on the surface, then etched away via a first mask to form a pair of first mask caps 41. The first mask caps 41 then are used as a mask for etching into the three poly-silicon layers 38-1, 40-1, 39-1 into two S-C-D columns. A first gate silicon dioxide dielectric layer 36-1 is then deposited all over the surface, including the top and sides of the S-C-D columns.

Please replace the third and fourth paragraphs of page 15 of the Disclosure currently on file with the following paragraphs:

The first mask caps 41 then are again used as a mask for etching back a thin layer from the gate electrode poly-silicon 37-1 and the gate dielectric columns 34-4. And the gate electrode interlayer dielectric 34-4 is again deposited on the whole surface then etched back to [[a]]an even level right above the first mask caps 41. As

such, the gate electrode poly-silicon 37-1 is surrounded by the gate dielectric 34-4 except at the surfaces facing the gate silicon dioxide dielectric 36-1. Then the first mask caps 41 are removed by etching onto the top of the S-C-D columns.

A sixth barrier metal 33-6 and a tungsten layer 32HIC (horizontal interconnect) are deposited in sequence by a CVD method. The tungsten layer 32HIC is etched back to [[a]]an even surface, then the seven barrier metal 33-7 is deposited all over the surface. Then through anisotroic etching via a photoresist mask into the three layers 33-6, 32HIC, and 33-7 to form a horizontal interconnect between one S-C-D column. Then the gate electrode interlayer dielectric 34-4 is deposited for the third time on the whole surface then etched back to a even level right above the seventh barrier metal 33-7.

Please replace the first paragraph of page 16 of the Disclosure currently on file with the following paragraph:

To look at the processing from a 3D perspective by taking Figure 2 at a partial cross-section plane II-II, Figure 8A shows an enlarged cross-sectional view of Q4 and the vertical interconnect 4' (or tungsten 32VIC-2). As mentioned, Q4 includes a source 6' (or poly-silicon [[38]]39-1), a gate electrode 1' (or poly-silicon 37-1), and a drain 5' (or poly-silicon [[39]]38-1). In particular, the silicon dioxide gate dielectric wall 36-1 is cylindrical. Figure 8B shows a 3D perspective view of the structure in Figure 8A, and Figure 8C shows a top view of the structure in Figure 8A. By looking at Figure 2 from a partial cross-section plane III-III, Figure 8D shows an enlarged side view of the gate electrode block 1' embedded with the S-C-D column of Q4 and a vertical interconnect column 4'.

Please replace the last paragraph of page 18 (continuing to page 19) of the Disclosure currently on file with the following paragraph:

The second embodiment can also be easily modified by shifting around the levels, the building blocks or their portions. As shown in Figure 17, a modified embodiment 2-1 chops off the top portion of the vertical interconnects 4, 4' in Figure

16 from the gate electrode 2 so as to reduce the manufacturing difficulty associated with long plugs. Alternatively, as discussed later in the seventh embodiment, the load transistors [[Q5, Q6]]may be eliminated from the second embodiment.

Please replace the fourth paragraph of page 22 of the Disclosure currently on file with the following paragraph:

The third embodiment can also be easily modified by shifting around the levels, the building blocks or their portions. For example, the whole level of Q1, Q2, and Vcc may be switched with the level of Q3, Q4, and Vss. Alternatively, as discussed later in the seventh embodiment, the load transistors [[Q5, Q6]]may be eliminated from the third embodiment.

Please replace the first paragraph of page 24 of the Disclosure currently on file with the following paragraph:

The fourth embodiment is hybrid of the first and third embodiments. This embodiment is obtained by substituting the bottom pair of vertical transistors in the third embodiment with a pair of horizontal transistor in the first embodiment. Referring to the circuit diagram in Figure 31 (exactly the same as Figure 23), a 6T vertical SRAM according to the fourth embodiment of the invention includes two transfer NMOS transistors Q5 and Q6 formed on the top of two load PMOS transistors Q1 and Q2, which are in turn formed on the top of two drive NMOS transistors Q3 and Q4 grown in the substrate. The levels of the load MOSs and the drive MOSs can be switched as long as the transfer MOSs stay within a shared gate electrode block. As shown in the 3D diagram of the fourth embodiment (Figure 32), Q1 includes a source 8, a gate electrode 2, and a drain 7. Q2 includes a source 8', a gate electrode 2', and a drain 7'. Q[[3]]5 includes a source 6, a gate electrode 16, and a drain 5. Q[[4]]6 includes a source 6', a gate electrode 16 and a drain 5'. Q[[5]]3, Q[[6]]4 (not shown) are constructed underneath the 3D structure shown in Figure 32.

Please replace the second paragraph of page 26 of the Disclosure currently on file with

the following paragraph:

The fourth embodiment can also be easily modified by shifting around the building blocks or their portions. As discussed later in the seventh embodiment, the load transistors [[Q5, Q6]]may be eliminated from the fourth embodiment.

Please replace the first paragraph of page 27 of the Disclosure currently on file with the following paragraph:

A pair of bit lines 9, 9' are connected to the top of Q5, Q6 such that no bit line contact is necessary. Each of the load transistors Q[[5]]1 and Q[[6]]2 includes an active region. A Vcc beam and a pair of horizontal interconnects 17, 17' are built above the [[in the]]horizontal transistors. The block [[1]]16 is embedded with the gate electrodes of Q5, Q6, and the word line 11 (shared gate/WL). Figure 40 shows a side view of the structure in Figure 39 looking from the plane of the front end of the word line 16 (G/WL).

Please replace the first paragraph of page 29 of the Disclosure currently on file with the following paragraph:

The fifth embodiment can also be easily modified by shifting around the building blocks or their portions. For example, the shared gate electrode block of Q5, Q6 may be shifted to the left side of Q3, Q4. As shown in Figure 45 the modified embodiment 5-1 extends the horizontal interconnect 3 to be as long as the horizontal interconnect 3'. As a result, the horizontal interconnect 3 also extends towards position 68 (Figure 46). The extension of the horizontal interconnect 3 evens the length of horizontal interconnects 3, 3', which results in more homogeneous SRAM properties. As discussed later in the seventh embodiment, the load transistors [[Q5, Q6]]may be eliminated from the fifth embodiment.

Please replace the last paragraph of page 29 (continuing to page 30) of the Disclosure currently on file with the following paragraph:

A pair of bit lines 9, 9' are connected to the top of Q5, Q6 such that no bit line contact is necessary. Each of the load transistors [[Q5, Q6]]includes an active region. A Vcc beam and a pair of horizontal interconnects 17, 17' are built above the horizontal transistors. The word line blocks 16, 16' are embedded with the gate electrodes of Q5, Q6 respectively. Figure 48 shows a side view of the structure in Figure 47 looking from the plane of the front end of the word line 16 (G/WL).

Please replace the first paragraph of page 30 of the Disclosure currently on file with the following paragraph:

The horizontal interconnect beam 17 connects Q[[6]]2 to the vertical interconnect column 4, and the horizontal interconnect beam 17' connects Q[[5]]1 the vertical interconnect column 4'. Above the drive transistors Q3 and Q4 are a pair of horizontal interconnect beams 3, 3' buried in an inter-layer insulating film. The horizontal interconnect beam 3 connects Q3 to the vertical interconnect column 4, and the horizontal interconnect beam 3' connect Q4 to the vertical interconnect column 4'. An additional pair of horizontal interconnects 3, 3' are provided in this embodiment than the fourth embodiment. The horizontal interconnect beam 3 connects Q6 to the vertical interconnect column 4, and the horizontal interconnect beam 3' connect Q5 to the vertical interconnect column 4'. Q3, Q4 are connected to one shared Vss beam 12, and Q1, Q2 are connected to a Vcc beam 13 with Vcc contacts 14, 14'. Thus, high integration and low-drive-voltage operation become possible.

Please replace the last paragraph of page 31 of the Disclosure currently on file with the following paragraph:

The sixth embodiment can also be easily modified by shifting around the building blocks or their portions. As discussed later in the seventh embodiment, the load transistors [[Q5, Q6]]may be eliminated from the six embodiment.